IN THE CLAIMS

Please amend the claims as follows:

Claims 1-13 (canceled)

Claim 14 (previously presented): A data latch circuit comprising:

a memory circuit which has first and second inverters having one output terminal connected to the other input terminal and the other output terminal connected to one input terminal and stores therein digital data which is a latch target;

first and second switch devices configured to switch and controlling whether a power supply voltage is supplied to said first and second inverters;

a third switch device configured to switch and controlling whether said digital data is inputted to said memory circuit; and

an output circuit configured to read digital data stored in said memory circuit,

said first and second switch devices being turned on in a period other than a cyclic sampling period to supply a power supply voltage to said first and second inverters,

said third switch device being turned on in said sampling period to input digital data to said memory circuit,

said output circuit having a passing electric current prevention unit which prevents a passing electric current to flow from a power supply terminal of said output terminal to a group terminal in said sampling period.

Claim 15 (original): The data latch circuit according to claim 14, wherein said output circuit outputs a signal having predetermined logic in said sampling period, and inverts and outputs data stored in said memory circuit in a period other than said sampling period.

Claim 16 (original): The data latch circuit according to claim 15, wherein said output circuit includes:

a first logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said first inverter in a period other than said sampling period; and

a second logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said second inverter in a period other than said sampling period.

Claim 17 (original): The data latch circuit according to claim 16, wherein said first and second logical operation circuits include any one of an NAND gate, an NOR gate and a clocked inverter.

Claim 18 (original): The data latch circuit according to claim 15, wherein to said output circuit are supplied a first signal indicating whether or not to be said sampling period and a second signal which has specific logic in a predetermined period other than said sampling period, and

said output circuit including:

a first logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said first inverter when said second signal has said specific logic in a period other than said sampling period; and

a second logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said second inverter when said second signal has said specific logic in a period other than said sampling period.

Claim 19 (original): The data latch circuit according to claim 18, wherein said first and second logical operation circuits include any one of an NAND gate, an NOR gate and a clocked inverter.

Claim 20 (previously presented): A liquid crystal display comprising:

signal lines and scanning lines being aligned;

display elements arranged in the vicinity of an intersection of said signal line and said scanning line;

a signal line drive circuit configured to drive each of said signal lines; and

a scanning line drive circuit configured to drive each of said scanning lines,

said signal line dive circuit including:

a shift register which has a plurality of register circuits and sequentially outputs shift register shift pulses shifted in synchronization with a clock signal;

a plurality of data latch circuits configured to latch digital data concerning pixel information in synchronization with each of said shift pulses;

a load latch circuit configured to simultaneously latch outputs from a plurality of said data latch circuits in synchronization with a load signal; and

a D/A converter circuit configured to convert a latch output from said load latch circuit into an analog pixel voltage to be then supplied to a corresponding signal line,

each of a plurality of said data latch circuits including:

a memory circuit which has first and second inverters having one output and being connected to the other input terminal and the other output terminal being connected to one input terminal, and stores therein digital data which is a latch target;

first and second switch devices configured to switch and controlling whether a power supply voltage is supplied to said first and second inverters;

a third switch device configured to switch and controlling whether said digital data is inputted to said memory circuit; and

an output circuit configured to read digital data stored in said memory circuit,

said first and second switch devices being turned on in a period other than a cyclic sampling period to supply a power supply voltage to said first and second inverters,

said third switch device being turned on in said sampling period to input digital data to said memory circuit,

said output circuit having a passing electric current prevention unit which prevents a passing electric current to flow from a power supply terminal of said output terminal to a group terminal in said sampling period.

Claim 21 (original): The data latch circuit according to claim 20, wherein said output circuit includes:

a first logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said first inverter in a period other than said sampling period; and

a second logical operation circuit which outputs a signal having predetermined logic in said sampling period, and inverts and outputs an output from said second inverter in a period other than said sampling period,

said first and second logical operation circuits being constituted by circuits which are equivalent to each other.